Design Guide for Xilinx FPGA Power Management Systems

1 Introduction

Field Programmable Gate Arrays (FPGAs) are a class of programmable logic devices based on an array of logic cells surrounded by a periphery of input/output cells. These IC's can be programmed in the field after manufacture in order to implement specific design functions.

The advanced technologies and smaller geometries used to fabricate the devices require increasingly lower supply voltages for the core voltage (typically 3.3, 2.5, 1.8, 1.5 and 1.2V). While the core supply voltage is decreasing, these devices must continue to support both newer and legacy interfaces, potentially requiring an I/O supply voltage which is different from the core voltage. Typical V_{ccio} voltages range from 1.2V up to 3.6V. Legacy applications may require a 5V I/O supply.

ST Microelectronics supports a complete power management solution for low and mixed-voltage FPGAs. This design guide serves to address the voltage and current requirements, including voltage sequencing, ramping, and current limiting. A list of regulators matching the minimum power supply requirement for Xilinx FPGA families is also included. The power requirements listed here are based on the most current information available. Designers should consult Xilinx's application literature for the up to date information.

2 Xilinx FPGA Requirements

2.1 Voltage Levels

Xilinx FPGAs require a supply voltage of 3.3, 2.5, 1.8, 1.5 and 1.2V for the core, depending on the specific family of FPGAs. The I/O voltage requirement depends on which I/O standards the FPGA is supporting. These voltages can range from 3.3V to 1.2V. The Virtex-4™, Virtex-II™, Virtex-II™ Pro and the Spartan-3™ also require an auxiliary voltage. The Xilinx core, auxiliary and I/O voltage requirements for each family are listed in the table below:

Xilinx FPGA Family	Core Voltage	Auxiliary Voltage	I/O Voltage
Virtex-4™	1.2V	2.5V	1.2V to 3.3V
Virtex-II Pro™	1.5V	2.5V	1.5V to 3.3V
Virtex-II™	1.5V	3.3V	1.5V to 3.3V
Virtex-E/EM™	1.8V	N/A	1.2V to 3.3V
Spartan-3™	1.2V	2.5V	1.2V to 3.3V
Spartan-3L™	1.2V	2.5V	1.2V to 3.3V
Spartan-3E™	1.2V	2.5V	1.2V to 3.3V
Spartan-IIE™	1.8V	N/A	1.2V to 3.3V
Spartan-II™	2.5V	N/A	1.5V to 3.3V

2.2 Power-On Requirements

At power-up, a minimum level of core supply current must be provided to the Xilinx FPGAs in order to properly power-up and configure. In addition, the core voltage V_{ccint} ramp time must be within a certain range, as specified in the datasheet for each family. The power supplies must also rise monotonically with a voltage droop less than 10mV/ms.
The power-up current and ramp time specifications for each family are as follows:

Xilinx FPGA Family	Min Power-Up Current (mA)			Ramp Time Specification
	Core	Aux	I/O	
Virtex-4™	Up to 850	500	N/A	200µs < T_{ccpo} < 50ms
Virtex-II Pro™	Up to 2200	250	100	200µs < T_{ccpo} < 50ms
Virtex-II™	Up to 1100	100	100	1ms < T_{ccpo} < 50ms
Virtex-E™	Up to 2000		100	2ms < T_{ccpo} < 50ms
Spartan-II™	250 – 2000		N/A	T_{ccpo} < 50ms
Spartan-IIE™	300 – 2000		N/A	2ms < T_{ccpo} < 50ms
Spartan-3™	55 – 340	N/A	N/A	no limit<Min Tcco< 2ms
Spartan-3L™	55 – 340	N/A	N/A	no limit<Min Tcco< 2ms
Spartan-3E™	55 – 340	N/A	N/A	no limit<Min Tcco< 2ms

N/A = Data currently non available

The following circuits address the power-on ramp up requirement, allowing for consistent and reliable power-up:

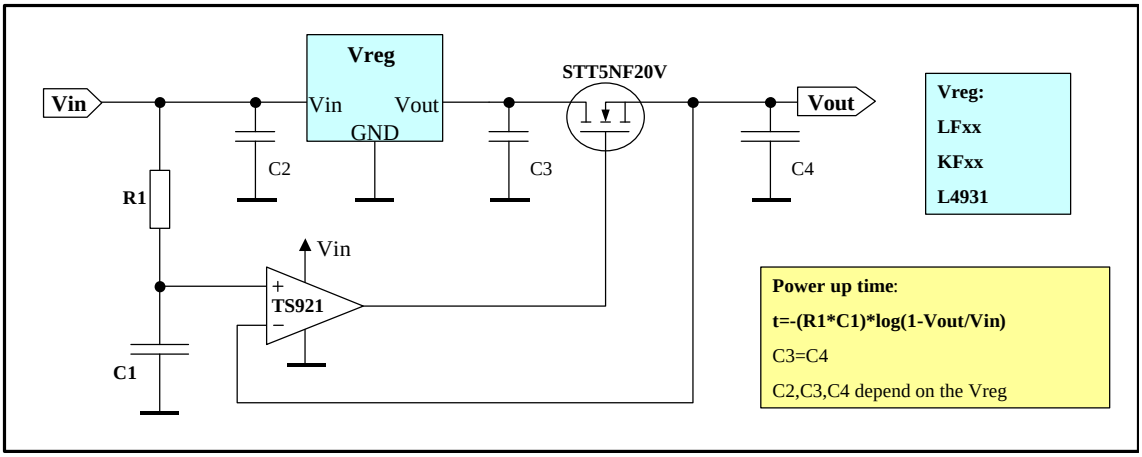


Fig 2.1- Power Up: Fixed output

The schematic in Figure 2.1 allows the designer to increase the output voltage slew rate of a fixed output Voltage Regulator. The MOSFET (STT5NF20V) acts as a pass element that is gradually switched on following the R1 and C1 charging time.

$$t=-(R1*C1)*\log(1-Vout/Vin)$$

Note: For this solution, the delta "Vin-Vout" must be higher than the Q1 V_{gs}

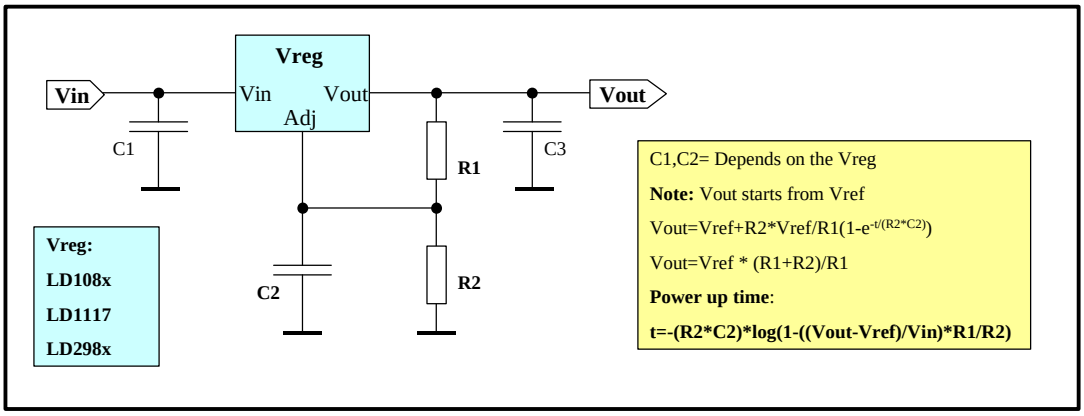


Fig 2.2 - Power Up: Adjustable Output LDO – Without GND pin

Using an adjustable Voltage regulator such as the **LD1085** or the **LD1117**, it is easy to implement a controlled output voltage slew rate. A capacitor (C2) is placed in parallel to the low side of the bridge resistor (R2), which is used to set the output voltage level.
Upon power up, the output of this circuit goes to the Vref (1.25V) then, from 1.25V to the set Vout

$$Vout=Vref * (R1+R2)/R1$$

It will follow the R2* C2 charging time as follows:

$$t=-(R2*C2)*log(1-((Vout-Vref)/Vin)*R1/R2)$$

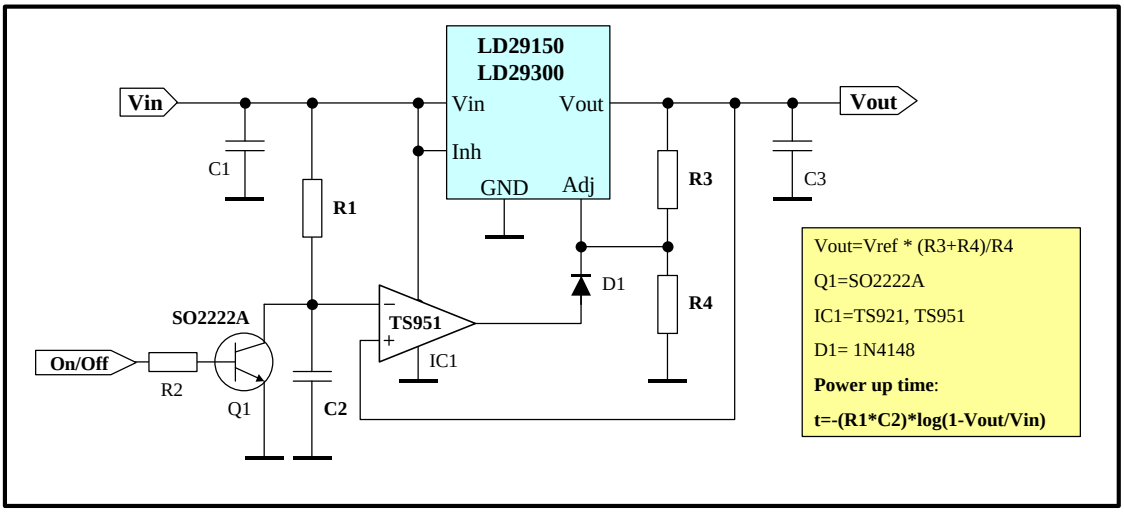


Fig 2.3 – Power Up: Adjustable Output LDO – With GND pin

The **LD29xxx** family offers the best solution to implement a controlled output voltage rise time.
Due to the internal voltage reference, which is referred to GND, it is possible to let the output voltage go from 0V to the set value (**Vout=Vref * (R3+R4)/R4**) according to the R1*C2 charging time.

$$T=-(R1*C2)*log(1-Vout/Vin)$$

2.3 Power Sequencing

The Virtex-II Pro™ family requires that the auxiliary power supply, V_{ccaux}, power up before or at the same time as V_{cco}. For the Virtex-II™, the power supplies can power up in any sequence, but if any V_{cco} bank powers up before V_{ccaux}, then each bank will draw up to 300mA until the V_{ccaux} supply powers up. (This does not harm the device.)

Powering up the core supply voltage before the I/O supply voltage is generally recommended for most FPGA families. When power sequencing is needed, the following circuit will control the power-up and power-down sequence of the Vcc_{core} and the V_{cco} supply voltages.

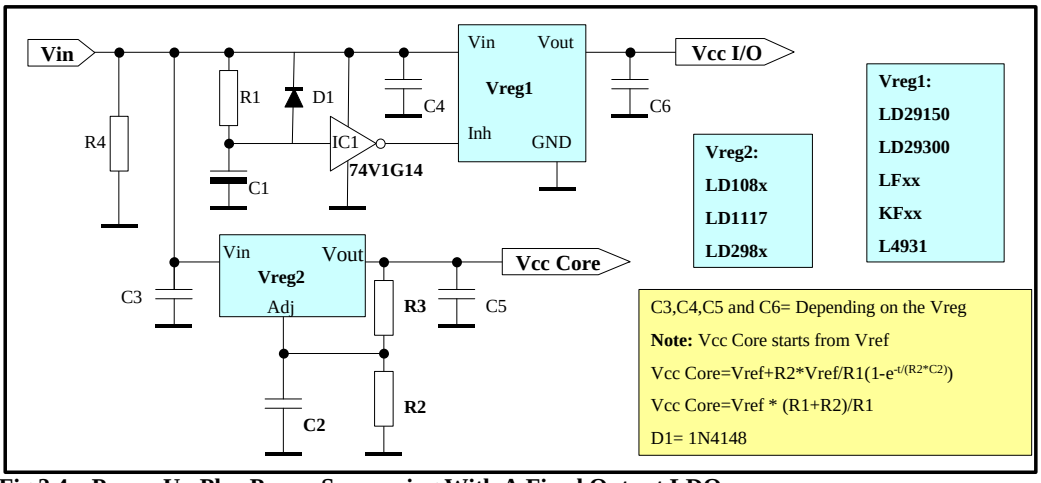


Fig 2.4 – Power Up Plus Power Sequencing With A Fixed Output LDO

Vreg2 powers-up the core with a slew rate controlled output voltage, due to R2 and C2

t=-(R2*C2)*log(1-((Vout-Vref)/Vin)*R3/R2)

The I/O section is powered through **Vreg1**, after a delay due to R1 and C1

t=-(R1*C1)*log(1-Vt"IC1"/Vin)

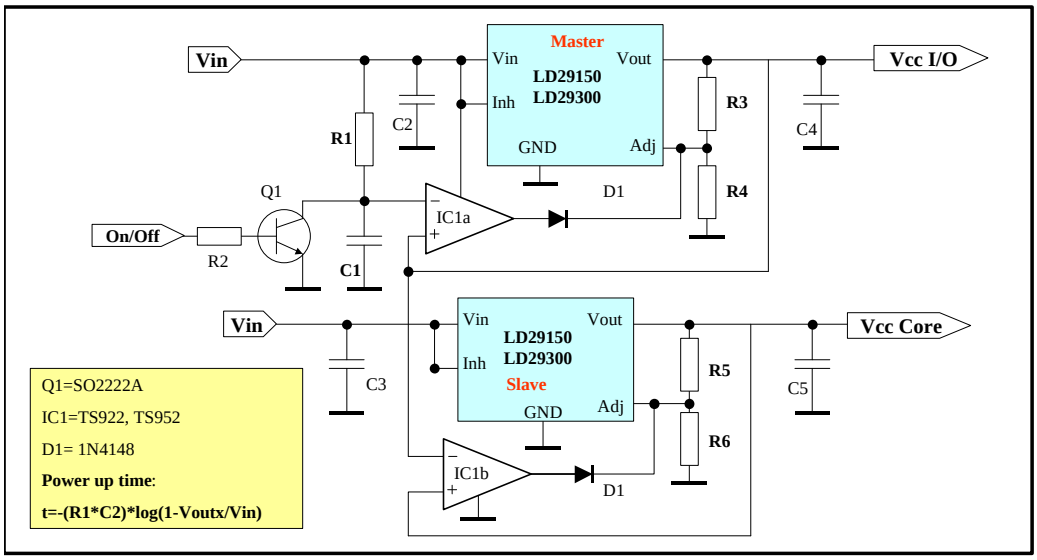


Fig 2.5 - Power Up Plus Power Sequencing With An Adj. Output LDO

This solution is suitable for those applications that require both a controlled slew rate on power up and power sequencing for the core and I/O voltages. Both outputs rise and fall with the same slew rate, set by R1 and C1. The different output voltage levels result in different power up times that create a power up sequence for the two supplies:

t=-(R1*C2)*log(1-Vccx/Vin)

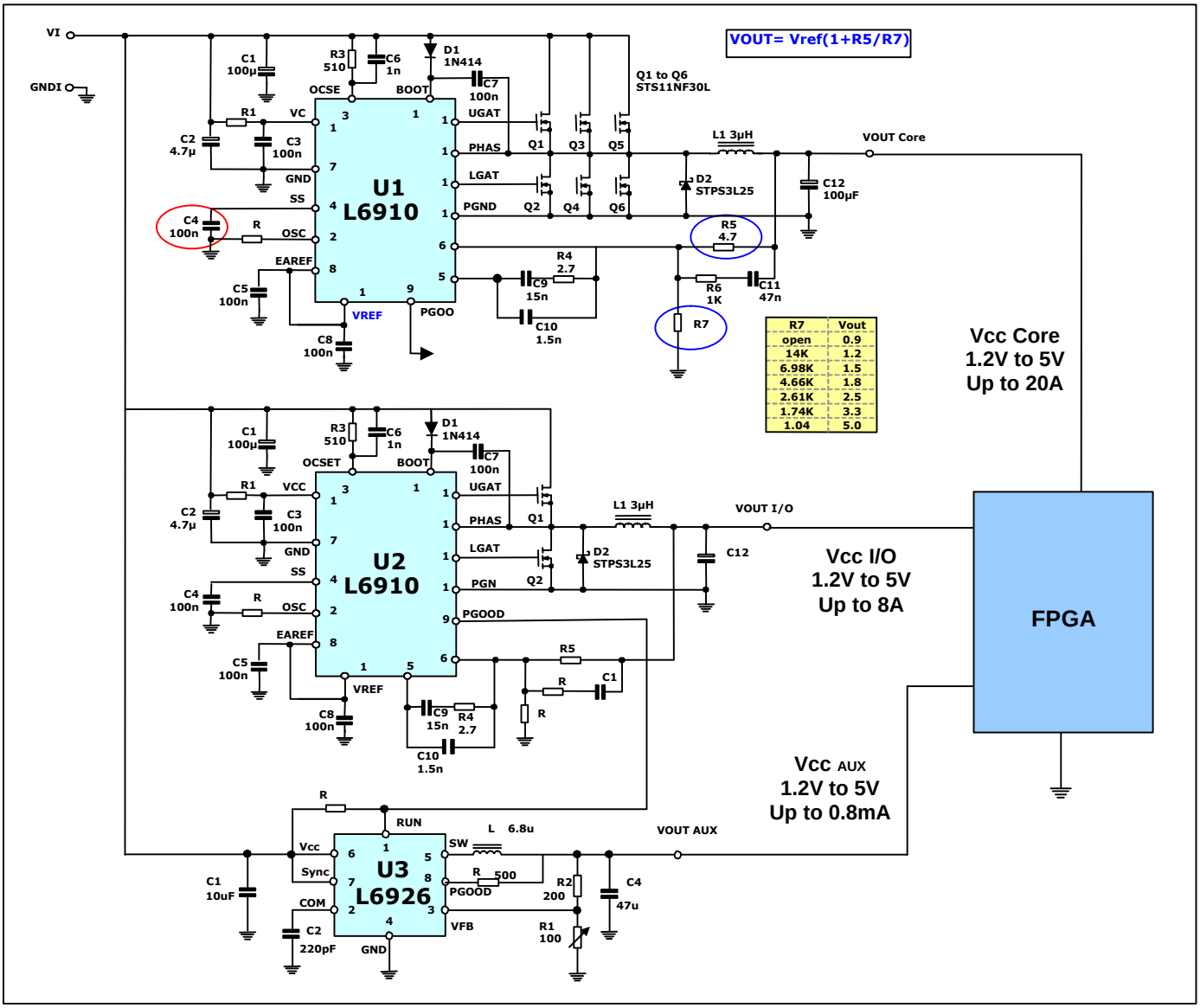
Note: Vout Master must be higher than Vout Slave

2.4 Higher Efficiency Solutions

A linear solution is usually easier and less expensive to implement but depending on the FPGA density and design, or the application requirement and available supply power, there are cases where either the current supply requirements can be higher that 3A or the voltage input is too high. Under those conditions the power dissipation across the linear regulator could became significant (between 2W and 3W). In other cases (such as in battery power applications) better efficiency is needed, and therefore linear solution is no longer suitable.
The following schematics are examples of switching solution that provide high efficiency performances

a) This solution is suitable for those applications using an FPGA such as Spartan-3™ or Virtex-II™, typically requiring:

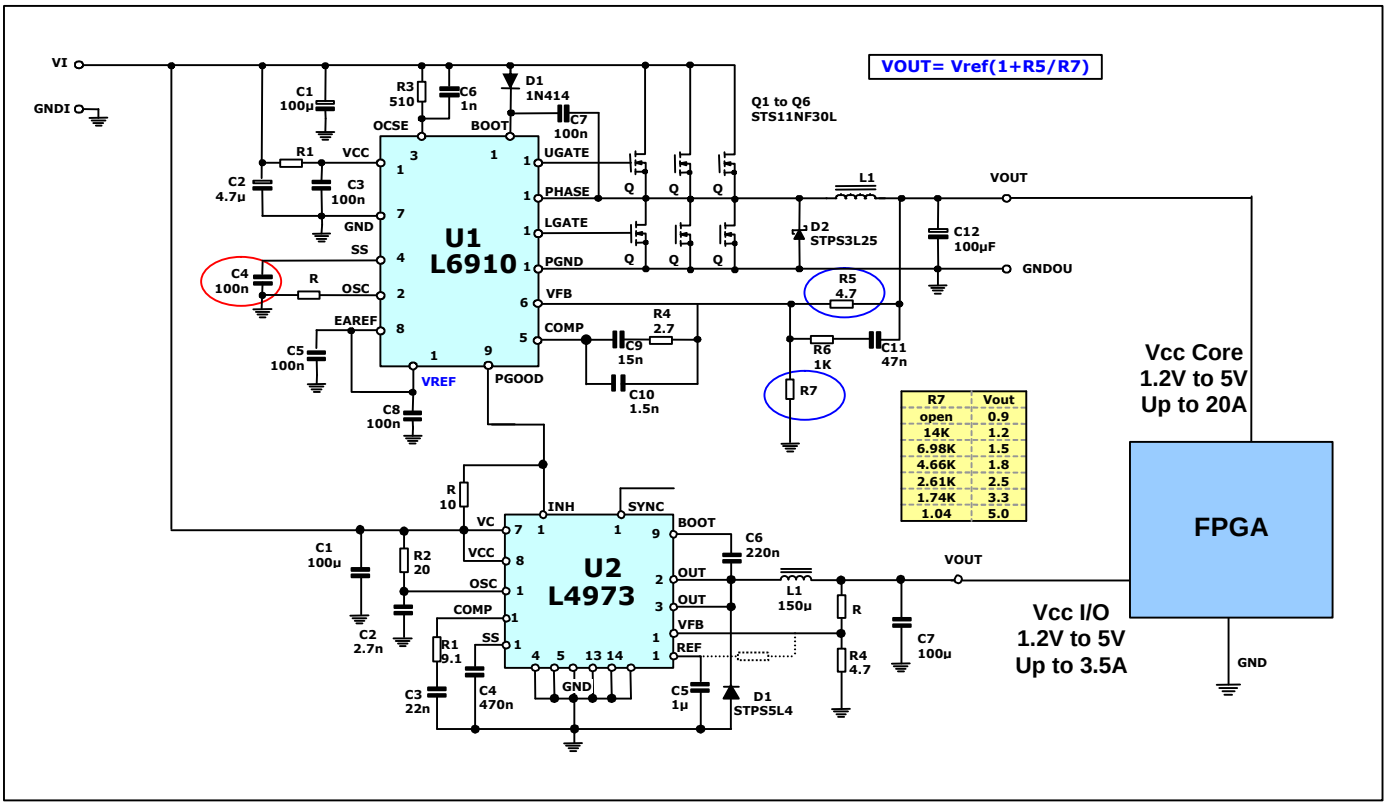
I. Core voltage range from 1.2V to 5V with a current capability up to 20A
II. I/O voltage from 1.2V to 5V with a current capability up to 8A
III. Auxiliary supply voltage form 1.2V to 5V up to 800mA



Thanks to the programmable soft start (by C4) and the power good feature of the L6910, the above circuit can be adapted to meet all the requirements of power-up and power sequencing.
If the Vaux section is not needed, the L6926 with its related circuitry can be omitted.

b) This solution is good for medium power requirements:

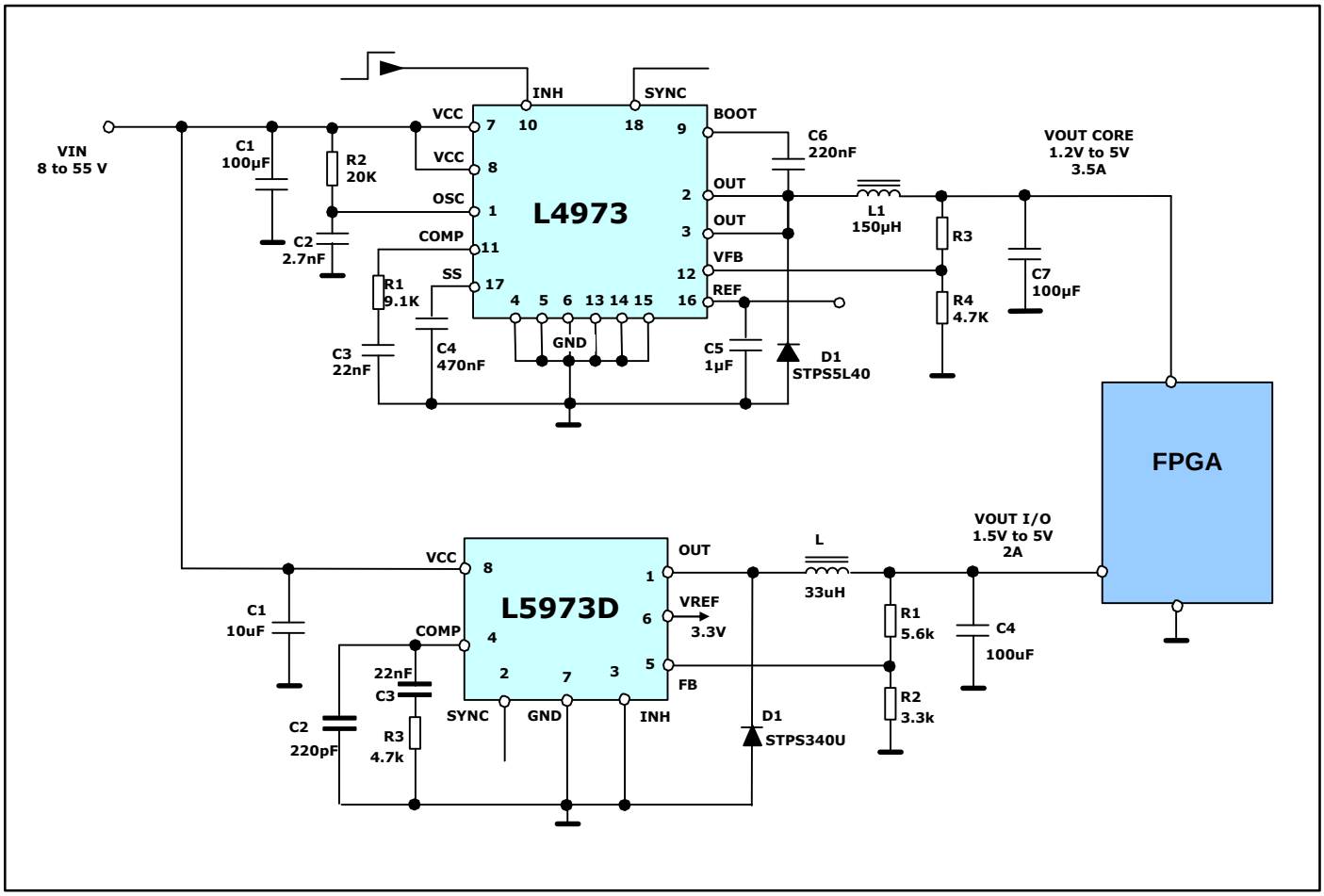
I. Core voltage range from 1.2V to 5V with a current capability up to 20A
II. I/O voltage from 1.2V to 5V with a current capability up to 3.5A



The number of MOSFETs depends on the core current requirements. For current up to 10A, only one MOSFET pair is necessary.

c) With a current lower than 4A the controller plus MOSFET solution can be replaced by a switching regulator, as showed on the schematic below

I. Core Voltage range from 1.2V to 5V with a current capability up to 3.5A
II. I/O voltage from 1.5V to 5V with a current capability up to 2A



2.5 Current Limiting

The Spartan-II™ and Spartan-IIE™ families require current limiting for situations where the circuit powered by the power supply exceeds a set current rating. During power-up, the Spartan-II™ and Spartan –IIE™ devices experience an in-rush current when the core voltage is between 0.6V and 0.8V. ST Microelectronics voltage regulators have internal current limiting features which limit the output of the devices once the output current has exceeded the limit. The output current limit can be found in the operating section of the ST Microelectronics voltage regulators datasheets.

2.6 Power Consumption Estimation

The power consumption of an FPGA depends on a number of different factors and is highly dependent on the design. Accurate power estimation methods must be used to ensure that a power supply system meets the FPGA's requirements for a given design. Xilinx provides a Web Power Estimator, available on their website, specifically for this purpose. This calculator considers design resource usage, toggle rates, operating clock frequencies, I/O usage and many other factors to generate the power estimation.

2.7 Suggested Xilinx FPGA Power Supply Solutions

The following table lists a few linear and switching voltage regulators suitable for each Xilinx FPGA. Those Vreg provide the minimum amount of supply current to insure proper device initialization during the power-on:

ST Microelectronics Voltage Regulators						
Xilinx Part Number	LINEAR			SWITCHING		
Virtex-4™	Vccint (1.2V)	Vccaux (2.5V)	Vcco[1]	Vccint (1.2V)	Vccaux (2.5V)	Vcco[1]
XC4VLX15, 25, 40	LD1117xx12	L4931ABD25x	L4931, LD29300	L6926D	ST750	L5972D
XC4VLX60, 80, 100	LD1117xx12	KF25	L4931, LD29300	L6926D	ST750	L5972D
XC4VLX160, 200	LD1117Axx12	LD29080 x25	L4931, LD29300	L5970	L6926D	L4973
XC4VSX25	LD1117xx12	L4931ABD25x	L4931, LD29300	L6926D	ST750	L5972D
XC4VSX35, 55	LD1117xx12	KF25	L4931, LD29300	L6926D	ST750	L5972D
XC4VFX12, 20, 40	LD1117xx12	L4931ABD25x	L4931, LD29300	L6926D	ST750	L5972D
XC4VFX60, 100	LD1117xx12	KF25	L4931, LD29300	L6926D	ST750	L5972D
XC4VFX140	LD1117Axx12	LD29080 x25	L4931, LD29300	L5970	L6926D	L4973
Virtex-II Pro™ Virtex-II Pro X™	Vccint (1.5V)	Vccaux (2.5V)	Vcco[1]	Vccint (1.5V)	Vccaux (2.5V)	Vcco[1]
XC2VP2, 4, 7	KF15	L4931ABD25x	L4931, LD29300	L6926D	ST750A	ST750A
XC2VP20, x20, 30	LD1117[2]	L4931ABD25x	L4931, LD29300	L5970D	ST750A	L5970
XC2VP40, 50,	LD29150xx15	L4931ABD25x	L4931, LD29300	L5972D	ST750A	L5970
XC2VP70, X70, 100, 125	LD29300xx15	L4931ABD25x	L4931, LD29300	L5973D	ST750A	L5970
Virtex-II™	Vccint (1.5V)	Vccaux (3.3)	Vcco[1]	Vccint (1.5)	Vccaux (3.3)	Vcco[1]
XC2V40 - XC2V1000	L4931ABD15TR	LD2981Cxx33	L4931, LD29300	L5970	ST763A	ST750A
XC2V1500 - XC2V3000	KF15	LD2981Cxx33	L4931, LD29300	ST1S03	ST763A	ST750A
XC2V4000, XC2V6000	LD1117[2]	LD2981Cxx33	L4931, LD29300	L4973	ST763A	ST750A
XCE2V8000	LD29150xx15	LD2981Cxx33	L4931, LD29300	L4973	ST763A	ST750A
Virtex-EM™ Virtex-E™	Vccint (1.8)		Vcco[1]	Vccint		Vcco[1]
XCV50E – XVC600E (Commercial grade)	LF18Cxx		L4931	L6926D or L5970D		ST750A
XCV812E – XCV200E (Commercial grade)	LD1117Axx18		L4931	L5970D		ST750A
XCV2600E - XCV3200 (Commercial grade)	LD1086xx18		L4931	L5972D		ST750A
XCV50E - XCV3200E (Industrial grade)	LD1085xx18		L4931	L5973D		ST750A

[1] The required I/O current will depend on several design specific factors, including I/O usage, loading, etc. Designers should use FPGA power estimator tools to determine the required Iccio current.

[2] The adjustable version of the LD1117 regulator can be configured to supply 1.5V.

ST Microelectronics Voltage Regulators						
Xilinx Part Number	*LINEAR*			*SWITCHING*		
Spartan-3™, Spartal-3L™ Spartan -3E™	**Vccint (1.2V)**	**Vccaux (2.5)**	**Vcco[1]**	**Vccint (1.2)**	**Vccaux (2.5V)**	**Vcco[1]**
XC3S50 – XCS1000	LD1117xx12	L4931xx25	Icc< 500mA LExx Icc< 1A LD1117A Icc< 1.5A LD29150 Icc< 3A LD29300 Icc< 5A LD1084	L5970	ST750A	Icc<450mA ST750A Icc< 1.0A L5970 Icc< 2.0A L5973 Icc< 3.5A L4973 Icc> 3.5A L6910
XC3S100E – XCS250E	LD1117xx12	L4931xx25		L5970	ST750A	
XC3S1000L – XC3S4000L	LD1117xx12	L4931xx25		L5970	ST750A	
XC3S1500 - XC3S5000	LD1117Axx12	L4931xx25		L4973	ST750A	
XC3S500E – XCS1600E	LD1117Axx12	L4931xx25		L4973	ST750A	
Spartan-IIE™	**Vccint (1.8V)**		**Vcco[1]**	**Vccint (1.8V)**		**Vcco[1]**
XC2S50E – XC2S300E (C) (Before PCN)[2]	LF18C (500mA)[4]		Icc< 500mA LExx Icc< 1A LD1117A Icc< 1.5A LD29150 Icc< 3A LD29300 Icc< 5A LD1084	L5970		Icc<450mA ST750A Icc< 1.0A L5970 Icc< 2.0A L5973 Icc< 3.5A L4973 Icc> 3.5A L6910
XC2S50E – XC2S300E (C) (After PCN)[2]	LF18C (300mA)[4]			ST750A		
XC2S400E – XC2S600E (C)	LF18C (500mA)[4]			L5970		
XC2S50E – XC2S300E (I) (Before PCN)[2]	LD1086xx18 (2A)[4]			L5973D or L4973		
XC2S50E – XC2S300E (C) (After PCN)[2]	LF18C (500mA)[4]			L5970		
XC2S400E – XC2S600E (I)	LD1117xx18 (700mA)[4]			L5970		
Spartan-II™	**Vccint (2.5V)**		**Vcco[1]**	**Vccint (2.5V)**		**Vcco[1]**
XC2S15 - XC2S 150 (I) (0°C < Tj) (data code 0321 or later)[3]	KF25xx (500mA)[4]		Icc< 500mA LExx Icc< 1A LD1117A Icc< 1.5A LD29150 Icc< 3A LD29300 Icc< 5A LD1084	L5970D		Icc<450mA ST750A Icc< 1.0A L5970 Icc< 2.0A L5973 Icc< 3.5A L4973 Icc> 3.5A L6910
XC2S15 - XC2S 150 (I) (Tj <0°C) (data code 0321 or later)[3]	LD29150xx25 (1.5A)[4]			L5972D		
XC2S15 - XC2S 150 (C) (data code 0321 or later)[3]	L4931 (250mA)[4]			ST750A		
XC2S15 - XC2S 150 (I) (0°C < Tj) (data code before 0321)[3]	KF25xx (500mA)[4]			L5970D		
XC2S15 - XC2S 150 (I) (Tj <0°C) (data code before 0321)[3]	LD29300xx25 (2A)[4]			L5972D		
XC2S15 - XC2S 150 (C) (data code before0321)[3]	KF25xx (500mA)[4]			L5970D		

[1] **The required I/O current will depend on several design specific factors, including I/O usage, loading, etc. Designers should use FPGA power estimator tools to determine the required Iccio current.**

[2] **Devices built after the Product Change Notice PCN 2002-05 (see http://www.xilinx.com/bvdocs/notifications/pcn2002-05.pdf) have improved power-on requirements. Devices after the PCN have a 'T' preceding the date code as referenced in the PCN. Note that the XC2S150E, XC2S400E, and XC2S600E always have this mark. Devices before the PCN have an 'S' preceding the date code. Note that devices before the PCN are measured with VCCINT and VCCO powering up simultaneously.**

[3] **The date code is printed on the top of the device's package.**

[4] **The minimum supply current ICCPO required for a successful power-on. If more current is available, the FPGA can consume more than ICCPO minimum, though this cannot adversely affect reliability.**

3 Summary

3.1 Supply Voltage Regulator Options

Xilinx power supply requirements for the core, I/O, and auxiliary power supplies include voltage outputs ranging from 1.2V to 5V and current outputs from tens of milliamps to multiple amperes. Depending on the system requirements, a linear or a switching regulator may be used to supply power to the FPGA. ST Microelectronics makes both linear and switching regulators with a wide variety of output voltages and output current levels. In selecting a voltage regulator for use in a Xilinx FPGA power supply design, it is important to understand the tradeoffs between linear and switching regulators.

Linear regulators are the best choice when board space is at a premium, low output noise is important or a fast response to inputs and transients is required. Linear regulators provide low to medium output currents with a simple design approach. An input capacitor is typically used to reduce the inductance and noise on the input to the LDO. The LDO also requires a capacitor on the output in order to handle system transients and to provide stability. ST Microelectronics offers voltage regulators (the LD298x and LD398x families) which allow low ESR ceramic capacitors to be used on the outputs, thereby reducing overall system cost. In addition, dual-output devices can be used to supply power for the core and I/O voltages in a single device. The ST2L05 offers fixed outputs in 1.5, 1.8, 2.5, 2.8, 3.0, 3.3V as well as an adjustable output option from 1.25V to 5.7V.

Switching regulators are best used when design efficiency is critical and/or large output currents are required. Switching supplies are known for excellent efficiency, but the output is more susceptible to noise due to the switching nature of the regulator. Switching regulators require inductors and input and output capacitors for DC-DC conversion.

3.2 Conclusion

The advancement of fabrication technologies and the shrinking of process geometries increase the complexity of the power management system required to supply the current generation of FPGAs. Today's FPGA designer must address the devices' specific voltage and current requirements including voltage sequencing, ramping, current limiting and power estimation. Designers must also choose which type of voltage regulator is best suited to their application. Depending on the system requirements, a linear or a switching regulator may be the best choice for powering the FPGA. ST Microelectronics makes both linear and switching regulators with a wide variety of output voltages and output current levels to provide complete power management solutions for Xilinx FPGAs.

Appendix A

The following table lists the output current for the recommended voltage regulators in this application note. Other regulators are also available, please consult your ST sales representative or the ST website, http://www.st.com, for the complete product portfolio.

ST Voltage Regulator Max Output Current

Part Number	Input Voltage	Output Voltage	Output Current	Topology	Evaluation board	On Line Simulation
LD2981	(Vout+1V) – 16V	1.5 – 5.0V	100mA	Linear		
L4931	3.3 - 20V	1.25 – 12V	250mA	Linear		
ST730A	5.2 – 11V	5V	450mA	Switching		
ST750A	4 – 11V	Adj.	450mA	Switching		
ST763A	3.3 – 11V	3.3V	500mA	Switching		
KFxx Series	2.5 – 20V	1.5V	500mA	Linear		
LF18	2.5 – 20V	1.8V	500mA	Linear		
KF25	2.5 – 20V	2.5V	500mA	Linear		
LD1117	2.4 – 15V	1.2 – 5.0V, Adj	800mA	Linear		
LD29080	2.5 – 13V	1.5 – 9V, Adj	800mA	Linear		
L6926D	2 – 5.5V	Adj (0.6 - 5V)	800mA	Switching	Yes	
L5970	4.4 – 36V	Adj (1.23 – 35V)	1A	Switching	Yes	Yes
LD1117A	2.5 -10V	1.2 – 5V, Adj	1A	Linear		
LD1086	4.1 - 30V	1.5 – 12V, Adj	1.5A	Linear		
LD29150	2.5 – 13V	1.5 – 8V, Adj	1.5A	Linear		
MC34063	3 – 40V	Adj	1.5A (switch current)	Switching		
ST1S03	3V to 16V	Adj down to 0.8V	1.5A	Switching	Yes	
L5972D	4.4 – 36V	Adj (1.235 – 35V)	2A (switch current)	Switching	Yes	Yes
L5973	4.4 – 36V	Adj (1.235 – 35V)	2.5A (switch current)	Switching	Yes	Yes
LD1085	2.85 – 30V	1.5 – 12V, Adj	3A	Linear		
LD29300	2.5 – 13V	1.5 – 9V, Adj	3.0A	Linear		
L4973	8 – 55V	Adj (0.5 – 50V)	3.5A	Switching	Yes	Yes
LD1084	3 – 30V	1.5 – 12V, Adj	5A	Linear		
L6910	5 – 12V	Adj (0.9 – 5V)	20A	Driver	Yes	

L497x & L597x On-Line Simulators

Besides support material such as application notes and evaluation boards, ST also provides online simulation software (“SW”) which can be accessed at:
http://www.st.com/stonline/products/support/designin/switchingl.htm
This software is dedicated to switching regulators up to 2A.